IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A radio frequency (RF) down/up-conversion circuit comprising:

a local oscillator chopping circuit comprising:

a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency-divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and

a multiplier capable of receiving said first and second LO signals and generating a ~~product signal of said first and second LO signals~~ signal that during selected periods of time has a signal polarity that is reversed relative to a signal polarity of said first LO signal; and

a differential radio frequency (RF) mixer having a first differential input port capable of receiving said ~~product~~ signal from said multiplier and a second differential input port capable of receiving a first differential modulated radio frequency (RF) signal and a second differential modulated radio frequency (RF) signal, wherein said differential RF mixer generates a differential output signal.

2. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 1 wherein said multiplier is an analog multiplier.

3. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 1 wherein said multiplier is an exclusive-OR gate.

4. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 1 wherein said differential output signal of said differential RF mixer is a double-sideband suppressed carrier signal.

5. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 4 further comprising a chopping switch capable of receiving said differential output signal of said differential RF mixer.

6. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 5 wherein said chopping switch is synchronized to said frequency divider such that said switching switch switches its internal connections at said LO/N frequency of said frequency divider and in tandem with said frequency divider.

7. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 1 wherein said differential RF mixer comprises a first differential pair of transistors comprising a first transistor and a second transistor, wherein a base of said first transistor is coupled to a first differential output signal received from said multiplier, and an emitter of said first transistor is coupled to an emitter of said second transistor and to said first differential modulated radio frequency (RF) signal.

8. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 7 wherein said differential RF mixer comprises a second differential pair of transistors comprising a third transistor and a fourth transistor, wherein a base of said third transistor is coupled to a second differential output signal received from said multiplier, and an emitter of said third transistor is coupled to an emitter of said fourth transistor and to said second differential modulated radio frequency (RF) signal.

9. (Original) The radio frequency down/up-conversion circuit as set forth in Claim 8 wherein a collector of said first transistor is coupled to a collector of said third transistor to form a first differential output signal of said differential output signal generated by said RF mixer and wherein a collector of said second transistor is coupled to a collector of said fourth transistor to form a second differential output signal of said differential output signal generated by said RF mixer.

10. (Currently Amended) A radio frequency (RF) receiver comprising:

a receiver front-end circuit capable of receiving an incoming RF signal from an antenna and filtering and amplifying said incoming RF signal; and

a radio frequency (RF) down/up-conversion circuit coupled to said receiver front-end circuit comprising:

a local oscillator chopping circuit comprising:

a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency-divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and

a multiplier capable of receiving said first and second LO signals and generating a ~~product signal of said first and second LO signals~~ signal that during selected periods of time has a signal polarity that is reversed relative to a signal polarity of said first LO signal; and

a differential radio frequency (RF) mixer having a first differential input port capable of receiving said ~~product~~ signal from said multiplier and a second differential input port capable of receiving a first differential modulated radio frequency (RF) signal and a second differential modulated radio frequency (RF) signal, wherein said differential RF mixer generates a differential output signal.

11. (Original) The radio frequency receiver as set forth in Claim 10 wherein said multiplier is an analog multiplier.

12. (Original) The radio frequency receiver as set forth in Claim 10 wherein said multiplier is an exclusive-OR gate.

13. (Original) The radio frequency receiver as set forth in Claim 10 wherein said differential output signal of said differential RF mixer is a double-sideband suppressed carrier signal.

14. (Original) The radio frequency receiver as set forth in Claim 13 further comprising a chopping switch capable of receiving said differential output signal of said differential RF mixer.

15. (Original) The radio frequency receiver as set forth in Claim 14 wherein said chopping switch is synchronized to said frequency divider such that said switching switch switches its internal connections at said LO/N frequency of said frequency divider and in tandem with said frequency divider.

16. (Original) The radio frequency receiver as set forth in Claim 10 wherein said differential RF mixer comprises a first differential pair of transistors comprising a first transistor and a second transistor, wherein a base of said first transistor is coupled to a first differential output signal received from said multiplier, and an emitter of said first transistor is coupled to an emitter

of said second transistor and to said first differential modulated radio frequency (RF) signal.

17. (Original) The radio frequency receiver as set forth in Claim 16 wherein said differential RF mixer comprises a second differential pair of transistors comprising a third transistor and a fourth transistor, wherein a base of said third transistor is coupled to a second differential output signal received from said multiplier, and an emitter of said third transistor is coupled to an emitter of said fourth transistor and to said second differential modulated radio frequency (RF) signal.

18. (Original) The radio frequency receiver as set forth in Claim 17 wherein a collector of said first transistor is coupled to a collector of said third transistor to form a first differential output signal of said differential output signal generated by said RF mixer and wherein a collector of said second transistor is coupled to a collector of said fourth transistor to form a second differential output signal of said differential output signal generated by said RF mixer.

19. (Currently Amended) A method of demodulating an incoming differential radio frequency (RF) signal having a frequency of RF comprising the steps of:

receiving a first local oscillator (LO) signal having a frequency of LO;

generating therefrom a frequency-divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with the first LO signal;

multiplying the first and second LO signals and generating a product signal of the first and second LO signals that during selected periods of time has a signal polarity that is reversed relative to a signal polarity of said first LO signal; and

mixing the product signal from the multiplier and the differential radio frequency signal and generating a differential output signal.

20. (Original) The method as set forth in Claim 19 wherein the differential output signal is a double-sideband suppressed carrier signal.